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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,053	02/21/2002	John Alan Miller	42P13415	5419

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EXAMINER	
COURTENAY III, ST JOHN	
ART UNIT	**PAPER NUMBER**
2194	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/081,053	MILLER ET AL.	
	Examiner	Art Unit	
	St. John Courtenay III	2126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-8,11,12,15-26,29 and 30* is/are rejected.

7)☒ Claim(s) *4,9,10,13,14,27 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

ST. JOHN COURTENAY III
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *April 24, 2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5-8, 11,12, 15-26, 29 and 30 are rejected under 35 U.S.C. § 102(e) as being anticipated by **Jourdan et al.** (U.S. Patent Application Publication US 2003/0120906).

Note: The cited '906 Jourdan reference constitutes a different inventive entity than the instant application although there is one common inventor (John Alan Miller).

As per independent claim 1:
Jourdan teaches a method comprising:

- maintaining first and second return buffers [see §0019, i.e, Address buffer 40 includes a Speculative (Return Stack Buffer) RSB 42 (SRSB 42), and a Committed RSB (CRSB 44)], for first and second instruction pipelines [see §0017, first level cache 12 and second level cache 14] respectively, both buffers having a plurality of return address entries [see §0019, i.e., "The return address buffer 40 stores predicted RETURN addresses and allows recovery of predicted RETURN addresses in the case of mis-predicted instruction fetching"

... "When a predicted return address stored in buffer 40 is popped by front-end 16, the predicted return address may come from either SRSB 42 or CRSB 44"]; and

- sending a request to the second instruction pipeline to fill the first return buffer with the entries in the second return buffer [e.g., see where the RETURN1 address is overwritten with the RETURN2 address in the Return Stack Buffer (RSB) and associated discussion §0018, beginning line 24].

As per independent claim 16:
Jourdan teaches an instruction pipeline in a microprocessor comprising:

- a decode unit, the decode unit to maintain a first return buffer having a plurality of return address entries [see §009, "The front end 16 of the processor 10 minimizes the time to decode instructions fetched from the target"]; and

- a branch prediction unit, the branch prediction unit to maintain a second return buffer and to fill the first return buffer with entries from the second return buffer [see §009, "branch prediction unit 28" and associated discussion; e.g., see where the RETURN1 address is overwritten with the RETURN2 address in the Return Stack Buffer (RSB) and associated discussion §0018, beginning line 24].

As per independent claim 23:
Jourdan teaches a method comprising:

- maintaining a return buffer for a decode unit, the return buffer having a plurality of return address entries [see §009,

i.e., "The front end 16 fetches and decodes instructions"; see also Return Stack Buffer (RSB) discussion beginning §0019, line 2];

- detecting a call instruction [see CALL instruction discussion §§0017, 0018];

- determining if the call instruction was detected by a branch prediction unit [see e.g., §0020: "SRSB 42 entries are updated when front-end 16 fetches a new CALL instruction and pushes a new predicted return address onto buffer 40 (typically, the predicted return address is the next instruction after the CALL instruction)"]; and

- sending a return address to the branch prediction unit if the call instruction was not detected by the branch prediction unit [see §009, "branch prediction unit 28" and associated discussion; e.g., see where the RETURN1 address is overwritten with the RETURN2 address in the Return Stack Buffer (RSB) and associated discussion §0018, beginning line 24].

As per dependent claim 2:
Jourdan teaches detecting a return instruction prior to sending a request to the second instruction pipeline to fill the first return buffer with the entries in the second return buffer [see, e.g., where the RETURN1 address is overwritten with the RETURN2 address in the Return Stack Buffer (RSB) and associated discussion §0018, beginning line 24].

As per dependent claim 3:
Jourdan teaches popping the first return buffer after detecting a return instruction [see e.g., "When a predicted return address

stored in buffer 40 is popped by front-end 16, the predicted return address may come from either SRSB 42 or CRSB 44" and associated discussion, §0019].

As per dependent claim 5:
Jourdan inherently teaches updating a pointer to the first return buffer after popping the first return buffer [see e.g., "When a predicted return address stored in buffer 40 is popped by front-end 16, the predicted return address may come from either SRSB 42 or CRSB 44" and associated discussion, §0019].

As per dependent claim 6:
Jourdan teaches detecting a call instruction prior to detecting a return instruction [see e.g., §0020: "SRSB 42 entries are updated when front-end 16 fetches a new CALL instruction and pushes a new predicted return address onto buffer 40 (typically, the predicted return address is the next instruction after the CALL instruction)"].

As per dependent claim 7:
Jourdan teaches pushing a return address corresponding to the call instruction onto the first return buffer after detecting a call instruction [see, e.g., §0019, "Address buffer 40 includes a Speculative RSB 42 (SRSB 42) and a Committed RSB (CRSB 44), both of which having multiple entries that may include predicted return addresses that have been pushed onto buffer 40 by front end 16"].

As per dependent claim 8:
Jourdan inherently teaches updating a pointer to the first return buffer after pushing the return address onto the first return buffer [see, e.g., §0019, "Address buffer 40 includes a Speculative RSB 42 (SRSB 42) and a Committed RSB (CRSB 44), both of which having multiple entries that may include predicted return

addresses that have been pushed onto buffer 40 by front end 16"].

As per dependent claim 11:
Jourdan teaches maintaining a first return buffer for a pipeline to translate instructions fetched from a memory device [see discussion §0010, i.e., "Instructions are fetched and decoded by a translation engine (not shown) and built into sequences of .mu.-ops called traces. These traces of .mu.-ops are stored in the trace cache 26"].

As per dependent claim 12:
Jourdan teaches maintaining a second return buffer for a pipeline that predicts branches in a cache [see e.g., "Address buffer 40 includes a Speculative RSB 42 (SRSB 42) and a Committed RSB (CRSB 44), both of which having multiple entries that may include predicted return addresses that have been pushed onto buffer 40 by front end 16" §0019].

As per dependent claim 15:
Jourdan teaches wherein the first and second return buffers are return stacks [see e.g., Return Stack Buffers (RSB) as discussed 019: "Address buffer 40 includes a Speculative RSB 42 (SRSB 42) and a Committed RSB (CRSB 44), both of which having multiple entries that may include predicted return addresses that have been pushed onto buffer 40 by front end 16"].

As per dependent claim 17:
Jourdan teaches the decode unit recognizes call instructions and return instructions [see §009, i.e., "The front end 16 fetches and decodes instructions"; see also CALL and RETURN instruction discussion §0018].

As per dependent claim 18:
Jourdan teaches the branch prediction unit to fill the first return buffer with entries from the second return buffer comprises the branch prediction unit to fill the first return buffer with entries from the second return buffer each time the decode unit recognizes a return instruction [e.g., see branch prediction discussion and associated CALL and RETURN instruction discussion §§0018, 0019; see §009, "branch prediction unit 28" and associated discussion].

As per dependent claim 19:
Jourdan teaches the decode unit sends a request to the branch prediction unit to fill the first return buffer with entries from the second return buffer each time the first return buffer is not full [e.g., see where the RETURN1 address is overwritten with the RETURN2 address in the Return Stack Buffer (RSB) and associated discussion §0018, beginning line 24; see also §009, i.e., "The front end 16 fetches and decodes instructions"; see also CALL and RETURN instruction discussion §0018; see branch prediction discussion and associated CALL and RETURN instruction discussion §§0018, 0019; see §009, "branch prediction unit 28" and associated discussion].

As per dependent claim 20:
Jourdan teaches a second branch prediction unit, the decode unit to send the second branch prediction unit a return address in the first return buffer if the decode unit recognizes a call instruction or a return instruction that the second branch prediction unit did not recognize [see e.g., see §009, "branch prediction unit 28" and associated discussion; see also §0018: "If the predicted path of execution for the return instruction is not correct (for example if an intervening branch instruction result is mis-predicted), RETURN1 address will be lost (it is no longer on RSB, having been over-written with RETURN2 address). Therefore, the next return instruction fetched will be mis-

predicted as having a RETURN2 address instead of the RETURN1 address"; see also §0019, "The return address buffer 40 stores predicted RETURN addresses and allows recovery of predicted RETURN addresses in the case of mis-predicted instruction fetching (as described above). Address buffer 40 includes a Speculative RSB 42 (SRSB 42) and a Committed RSB (CRSB 44), both of which having multiple entries that may include predicted return addresses that have been pushed onto buffer 40 by front end 16. When a predicted return address stored in buffer 40 is popped by front-end 16, the predicted return address may come from either SRSB 42 or CRSB 44"].

As per dependent claims 21, 22:
Jourdan teaches the branch prediction unit comprises a cache branch prediction unit to predict branches in a cache, and notification of a cache miss, as claimed [e.g., see §0017, cache 12 and cache 14; also see branch prediction discussion §§0018-0020; see §009, "branch prediction unit 28" and associated discussion].

As per dependent claim 24:
See the rejection of claim 7 above.

As per dependent claim 25:
Jourdan teaches detecting a return instruction [see e.g., RETURN1 and RETURN2 discussion, §0018].

As per dependent claim 26:
Jourdan teaches popping a return address from the return stack buffer [see e.g., "When a predicted return address stored in buffer 40 is popped by front-end 16, the predicted return address may come from either SRSB 42 or CRSB 44, §0019].

As per dependent claim 29:

See the rejection of claim 21 above [e.g., see discussion §§ 0017-0020].

As per dependent claim 30:
Jourdan teaches determining if the return instruction was detected by the branch prediction unit and sending a return address in the return buffer to the branch prediction unit if the return instruction was not detected by the branch prediction unit [see §009, "branch prediction unit 28" and associated discussion; e.g., see where the RETURN1 address is overwritten with the RETURN2 address in the Return Stack Buffer (RSB) and associated discussion §0018, beginning line 24].

Indication of Allowable Subject Matter:
Dependent claims 4, 9, 10, 13, 14, 27 and 28 appear to be allowable over the prior art of record if rewritten to include all of the limitations of the base claim and any intervening claims, subject to the results of a final search. These claims stand objected to as being dependent upon a rejected base claim.

As per dependent claims 4, 10:
The prior art of record does not teach, nor fairly suggest the step of determining if the return instruction was detected by a third instruction pipeline and sending a return address in the first return buffer to the third instruction pipeline if the return instruction was not detected by the third instruction pipeline, as claimed.

As per dependent claim 9:
The prior art of record does not teach, nor fairly suggest the step of determining if the call instruction was detected by a third instruction pipeline and sending a return address in the first

return buffer to the third instruction pipeline if the call instruction was not detected by the third instruction pipeline, as claimed.

As per dependent claims 13, 14, 27, 28:
The prior art of record does not teach, nor fairly suggest the step wherein each entry in the return buffer comprises a valid bit that indicates whether the corresponding return address is valid, as claimed.

Prior Art not relied upon:
Please refer to the references listed on the attached PTO-892 which are not relied upon in the claim rejections detailed above.

How to Contact the Examiner:

Any inquiry concerning this communication or earlier communications from the examiner should be directed to St. John Courtenay III, whose telephone number is 571-272-3761. A voice mail service is also available at this number. The Examiner can normally be reached on Monday - Friday, 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, An Meng-AI who can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

All responses sent by U.S. Mail should be mailed to:

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

PTO CENTRAL FAX NUMBER:
703-872-9306

- Any inquiry of a general nature or relating to the status of this application should be directed to the **TC 2100 Group receptionist: (571) 272-2100.**

ST. JOHN COURTENAY III
PRIMARY EXAMINER